WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a substrate;

an insulating layer formed on the substrate;

a fin formed on the insulating layer;

silicided source and drain regions formed adjacent the fin; and

a metal gate formed over a portion of the fin.

2. The semiconductor device of claim 1 wherein fin includes silicon.

3. The semiconductor device of claim 1, wherein the metal gate includes tantalum or titanium.

4. The semiconductor device of claim 1, further comprising:

at least one dielectric layer formed between the fin and the metal gate.

5. The semiconductor device of claim 1, wherein the silicided source and drain regions of the fin are fully silicided down to the insulating layer.

6. The semiconductor device of claim 5, wherein the silicided source and drain regions have a thickness ranging from about 400 Å to about 1500 Å.

7. The semiconductor device of claim 1, further comprising:

a pair of spacers formed over portions of the fin and on opposite sides of the metal gate.

8. The semiconductor device of claim 7, wherein the portions of the fin under the pair of spacers separate a channel region of the fin from the silicided source and drain regions.

9. A method of manufacturing a semiconductor device, comprising:

forming a fin structure on an insulator;

forming source and drain regions;

forming a gate structure over a channel portion of the fin structure;

forming a dielectric layer adjacent the gate structure;

removing material in the gate structure to define a gate recess in the dielectric layer;

forming a metal gate in the gate recess; and

siliciding the source and drain regions.

10. The method of claim 9, wherein the forming a gate structure includes:

depositing a gate material over the fin structure, and

selectively etching the gate material to define a dummy gate.

11. The method of claim 10, further comprising:

forming a plurality of spacers adjacent the dummy gate.

12. The method of claim 11, wherein the removing material in the gate structure includes:

removing the dummy gate.

13. The method of claim 9, wherein the forming a dielectric layer includes:

depositing a dielectric material over the gate structure, and

polishing the dielectric material until a top surface of the dielectric material is coplanar with a top surface of the gate structure and the top surface of the gate structure is exposed.

14. The method of claim 9, further comprising, before the siliciding the source and drain regions:

removing the dielectric layer.

15. The method of claim 9, wherein the siliciding the source and drain regions includes:

depositing a metal on the source and drain regions, and

annealing the metal to fully silicide the source and drain regions.

16. A semiconductor device, comprising:

a substrate;

an insulating layer formed on the substrate;

a fin formed on the insulating layer;

a dielectric layer formed on the fin;

a metal gate formed over a portion of the fin and the dielectric layer;

a pair of spacers formed on the fin on opposite sides of the metal gate; and

silicided source and drain regions formed on the opposite sides of the metal gate.

17. The semiconductor device of claim 16, wherein the metal gate includes tantalum or titanium.

18. The semiconductor device of claim 16, wherein the silicided source and drain regions are composed of silicide down to the insulating layer.

19. The semiconductor device of claim 16, wherein the metal gate and the pair of spacers are located over a channel region of the fin, and

wherein the silicided source and drain regions comprise a silicide material down to the insulating layer.

20. The semiconductor device of claim 19, wherein a thickness of silicided source and drain regions ranges from about 400 Å to about 1500 Å.